

RZ/G1M Starter Kit Board Hardware Manual

YR8A77430HA02BG
(Platform version device)

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Revision History	RZ/G1M Starter Kit Board Hardware Manual
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Revision	Date	Description	
		Page	Modification
1.00	Dec. 2017	-	First revision issued.

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1. Overview

The RZ/G1M is a new generation product featuring the functionality required for the Human Machine Interface systems. Its newly employed bus configuration maximizes system performance, space saving, and cost efficiency.

The RZ/G1M Starter Kit Board, is an RZ/G1M-specific evaluation board that can be used to evaluate solutions using the RZ/G1M and to develop operating systems, device drivers, and applications. Using the RZ/G1M Starter Kit Board allows the developers to efficiently conduct required tasks such as evaluation of the RZ/G1M system performance and thus greatly reduces the turn-around time in product development.

1.1. Features

1.1.1. The RZ/G1M includes:

- Two 1.5-GHz ARM Cortex™-A15 MPCore™ cores (dual core: option)
- Memory controller for DDR3-SDRAM (DDR3-1600) with 32 bits × 2 channel
- Three-dimensional graphics engines
- Video processing unit
- Sound processing unit
- SD card host interface (3 channels), MMCIF (1 channel)
- USB2.0 host (1 channel), USB2.0 host/function (1 channel)
- DU (digital RGB 2 channels), DCU, TCON, VIN (2 channels)
- VSP1, VCP3, FDP1, 2D-DMAC
- SCU, SSIU (10 channels), ADG
- CAN, Ethernet MAC, Ethernet AVB
- WDT, TPU, CMT1, TMU, CPG, INTC, DMAC, LBSC
- I²C (5 channels), IIC (2 channels), SCIF (6 channels), SCIFA (6 channels), SCIFB (3 channels), MSIOF (3 channels), QSPI, HSCIF (3 channels), PWM (7 channels)
- GPIO, etc
- Power supply voltages (typ.) 3.3 V, 1.8 V, 1.5 V/1.35 V, 1.0 V

1.1.2. The RZ/G1M Starter Kit Board includes:

Table 1.1.1 List of RZ/G1M Starter Kit Board Functions (1)

RZ/G1M Starter Kit Board Function List. Page 1 of 2			
Board Function	Module	Description	Note
RAM	DDR3	Dual Channel DDR3L-1600, 1GByte x2 channels, 32bit data width x2 channels 4Gbit(16bit data width) x4 devices. SDRAM Backup feature: Not Supported.	Hynix H5TC4G63AFR-PBA x4
	LBSC	No device.	
ROM	LBSC	No device.	Pin Multi: QSPI
	QSPI	two SPI Flash on board. Spansion S25FL512SAGMFIG11 (512Mbit=64MB) x1 Spansion S25FL032P0XMF1011 (32Mbit=4MB) x1	Pin Multi: LBSC_A[25:20] Related Jumper: JP2
Debug I/F	DBG	Connector: HTST-110-01-S-DV (20pin)	
	DBG2	---	not supported
	GPIO	LED x3 devices 'GPLED' for General Purpose. LED2~LED4 Mechanical switch x3 elements 'TactSW' for General Purpose.	GPIOs: GP2_19~GP2_21 GPIOs: GP7_0~GP7_2
	SCIF0	Debug Serial x1 (TX, RX) USB to UART Bridge SILICON LABS CP2102-GM x1 (Bridge spec: max 1Mbps) Connector: USB Type miniAB	
	SCIF1	---	not supported
LAN	EtherMAC	Debug Ether(100Mbps) RMII PHY: MICREL KSZ8041RNL1 Connector: CN10 CWKRJ-13BNL EXIO Connector B (CN3 : QSH-030-01-L-D-A-K)	For Interrupt: IRQ0 For Reset: GP5_22 (AVB_TXD4) Pin Multi: EtherAVB
SATA I/F	SATA0	3Gbps, Gen2 Connector: CN4: HSAT-M07-V5D-40	Pin Multi: USB3.0
PCIE I/F	PCI express	PCI Express Base Specification Revision 2.0, 1-lane, 2.5GT/s or 5.0GT/s Connector: CN5: JPCIE-4CEE36XRT110	Pin Multi: SATA1
USB2.0 I/F	USB2.0 ch0	USB2.0 Host or Function Connector: Type miniAB.	
	USB2.0 ch1	USB2.0 Host Connector: Type A.	
SDHI	SDHI0	Connector: SD Card slot. Interface voltage: Either 3.3V or 1.8V.	For voltage control: GP2_12
	SDHI1	---	not supported
	SDHI2	Connector: microSD Card slot. DBG3 can be connected instead of microSD card. Interface voltage: Either 3.3V or 1.8V.	For voltage control: GP2_26 Pin Multi: MMC
Video Output	DU0_LVDS	LVDS output. 5 pair (CLK, CH0~CH3) Connector: Signal: Hirose CN30: DF14A-20P-1.25H(55), TouchScreen: CN31: JW-XH250S-10-K	For Interrupt: IRQ1
	DU1	HDMI output HDMI Transmitter.ADV7511WBSWZ Connector: Type A Receptacle: CN45:Accurate Innotech HMNF-195N-4BH90	For Interrupt: GP3_29 (DU1_ODDF_3)
Video Input	VIN0	YCbCr 8bit. BT656 Video Decoder: Analog Devices ADV7180WBCP32Z, Connector: CN15 RCA compite Video	For Interrupt:
	VIN1	Connector: EXIO Connector B (CN3 :QSH-030-01-L-D-A-K)	Pin Multi: EtherAVB

Table 1.1.2 List of RZ/G1M Starter Kit Board Functions (2)

RZ/G1M Starter Kit Board Function List. Page 2 of 2			
Board Function	Module	Description	Note
Audio	SSI0, SSI1, SSI2, SSI9	Either [A] or [B] [A] Audio Output (SSI0), Input (SSI1) Codec: AKM AK4642EN x1 Connector: mini jack x1 for stereo line output Connector: mini jack x1 for stereo line/MIC input [B] Audio Multi-Channel Output (SSI0, SSI1, SSI2, SSI9) HDMI Transmitter ADV7511WBSWZ Connector: HDMI standard type A	Note: SSI channels connected to AK4642EN can be selected by 0Ω resistor. (Initial setting) Related Jumper: JP3
	SSI3, SSI4	EXIO Connector A (CN23 : QSE-060-01-F-D-A)	Note: Connect to CN23 as GPIO2_9,10,11,14
	SSI5, SSI6	EXIO Connector A (CN23 : QSE-060-01-F-D-A)	Note: Connect to CN23 as GPIO2_15,16,17,18
CAN	RCAN	CN11 : JW-XH250S-03-K This interface is connected to the following devices. CAN transceiver Maxim MAX3051 (3.3V)	Related Jumper: JP4
I ² C I/F	I ² C1	Interface voltage: 3.3V This interface is connected to the following devices. PMIC DA9063 (Alternative/HS-I2C)	
	I ² C2	Interface voltage: 3.3V This interface is connected to the following devices. HDMI Transmitter ADV7511, Video decoder ADV7180, Audio codec AK4642, (I2C EEPROM)	
	I ² C4	Interface voltage: 3.3V This interface is connected to the following devices. Pin header (CN31 : JW-XH250S-10-K)	Note: for LCD touch panel control.
	I ² C5	Interface voltage: 1.8V EXIO Connector A (CN23 : QSE-060-01-F-D-A)	
	I ² C6	Interface voltage: 1.8V This interface is connected to the following devices. PMIC DA9063, DA9210 (PM-I2C)	
EXIO Connector	various modules	EXIO Connector A CN23 samtec 120pin.QSE-060-01-F-D-A EXIO Connector B CN3 (for EtherAVB or VIN1) samtec 60pin.QSH-030-01-L-D-A-K	
Power IC	—	International Rectifier: IR3838MPbF (12V->5V) Dialog Semiconductor DA9210 (5V-> DVFS_1.0V, Core_1.0V) Dialog Semiconductor DA9063 (5V-> 3.3V, 1.8V, 1.35V, Vtt, SDHI0 and SDHI2 power) Diodes Incorporated: ZLDO1117G12TA (3.3V->1.2V)	2.5V not supported.
Power Supply	—	DC12.0V input	
Board size	—	170mm x 125mm	

1.2. Usage Notes

1.2.1. RZ/G1M Starter Kit Board Specifications

- Take particular care to ensure the correct configurations of the jumpers and switches mounted on the RZ/G1M Starter Kit Board. Incorrect configurations may damage on-board devices.
- For the RZ/G1M Starter Kit Board, be sure to use the power supply that comes with it. Applying a voltage greater than 12 V may damage devices on the RZ/G1M Starter Kit Board.
- There are sequences for turning on and off the power supply to the RZ/G1M. For the RZ/G1M Starter Kit Board, be sure to obey the notes below.

(1) When power is turned on

Be sure to confirm that the ACC switch (SW26) is off before plugging the AC adapter into the power source.

It is prohibited to plug the AC adapter into a power source while the ACC switch (SW26) is on.

(2) When power is shut off

Be sure to turn off the ACC switch (SW26) before unplugging the AC adapter from the power source.

It is prohibited to unplug the AC adapter from the power source while the ACC switch (SW26) is on.

- The maximum current draw for the VSYS and D5.0V pins on the RZ/G1M Starter Kit Board is 7A each. Therefore, operation should be such that the current drawn by either pin does not exceed 7A. Also ensure that the current draw does not exceed 7A if an IO expansion board or external storage device is connected to the RZ/G1M Starter Kit Board.

1.3. Board Configuration

The RZ/G1M Starter Kit Board is composed of a single board whose size is 170 mm × 125 mm.
Figure 1.3.1 shows a block diagram of the RZ/G1M Starter Kit Board.

1.3.1. Block Diagram of RZ/G1M Starter Kit Board

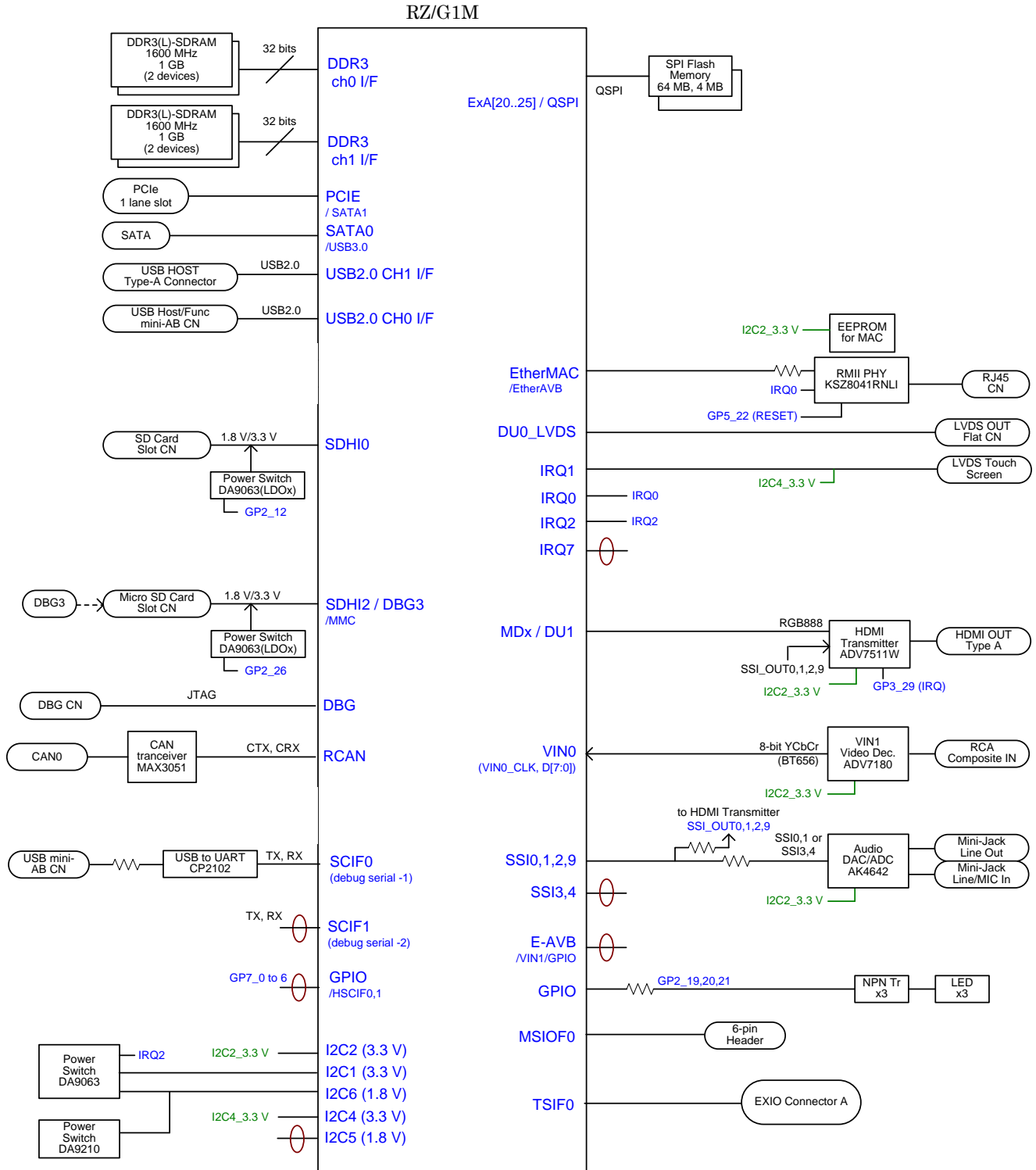


Figure 1.3.1 Block Diagram of RZ/G1M Starter Kit Board

1.3.2. Address Map of RZ/G1M Starter Kit Board

For the DDR3L memory space, see the section DDR3L-SDRAM Interface.

For other address space, see the Hardware section in the RZ/G Series User's Manual

2. RZ/G1M Starter Kit Board Interface Module Specifications

2.1. Mode Setting

2.1.1. Specifications

The operating mode of the RZ/G1M is set by a power-on reset. Each of the mode pins is set by pull up or pull down resistors, mounted on the development board. Several may also be changed by jumpers. For details on each operating mode, see the documents related to the RZ/G1M operating mode specifications.

2.1.1.1. MD0 Pin — Selection of Free-Running Mode or Step-Up Mode²

This pin selects the free-running mode or step-up mode.

MD0	Free-Running Mode or Step-Up Mode
0	Free-running mode (Fixed)
1	Step-up mode

2.1.1.2. MD[3:1] Pins — Selection of Boot Device

These pins select the boot device.

MD3	MD2	MD1	Selection of Boot Device
0	0	0	Boot from area 0 (boot from the external mask ROM)
0	1	0	QSPI (48.75 MHz/16-Kbyte transfer) (Fixed)
0	0	1	Reserved
0	1	1	Reserved
1	0	0	QSPI (39 MHz/16-Kbyte transfer)
1	0	1	Reserved
1	1	0	QSPI (39 MHz/4-Kbyte transfer)
1	1	1	Reserved

2.1.1.3. MD4 Pin — Selection of CS0 Space Size

This pin selects whether the area 0 space (CS0) is used as a normal space (64 Mbytes) or an expanded space (128 Mbytes).

MD4	Area Division
0	Area 0: 64 Mbytes (Fixed.... Area0 not used)
1	Area 0: 128 Mbytes

2.1.1.4. MD5 Pin — Selection of Secure or Non-Secure Mode

This pin selects the secure or non-secure mode

MD5	Selection of Secure or Non-Secure Mode
0	Secure (When LCS = Secure, the value read from the register for MD5 is forcibly set to 0.)
1	Non-secure (Default)

2.1.1.5. MD[7:6] Pins — Selection of Master Boot Processor

These pins select the master boot processor.

MD7	MD6	Selection of Master Boot Processor
0	0	CA15 boot (Fixed)
0	1	Reserved
1	0	SH boot (32 bits)
1	1	Reserved

2.1.1.6. MD8 Pin — Selection of Area 0 Space Data Bus Width

This pin sets the data bus width of the area 0 space (CS0) to 8 bits or 16 bits. Select the data bus width of the boot device connected to the LBSC.

MD8	EXBUS Area 0 Data Bus Width
0	8-bit bus (Fixed.... Area0 not used)
1	16-bit bus

2.1.1.7. MD9 Pin — Selection of Crystal Resonator or Crystal Oscillator

This pin selects either a crystal resonator or a crystal oscillator to be connected to the EXTAL/XTAL pins. A crystal oscillator (X6: 20 MHz) is mounted on the RZ/G1M Starter Kit Board by default. The crystal resonator (X5) and its peripheral circuit are not mounted.

MD9	EXTAL/XTAL Pin Setting
0	An external clock is input to the EXTAL pin. (Fixed)
1	A crystal resonator is connected to the EXTAL and XTAL pins.

2.1.1.8. MD12 — Reserved

Do not change the initial setting at shipment (MD12 = 0).

2.1.1.9. MD21, MD20, MD11, MD10, and MDT[1:0] Pins — Switching of JTAG, SDHI1, and SDHI2

These pins select the debugging function through the JTAG connector (CN1) or the SD card slot. Debugging through SDHI1 or SDHI2 is possible by the combination of MD pin settings in the RZ/G1M specifications, but not available on the RZ/G1M Starter Kit Board.

MD10	MD[21:20]	MD11	MDT[1:0]	JTAG	SDHI1	SDHI2
0	00	-	--	Boundary scan	Normal function	Normal function
0	10	0	--	Coresight (*1)	Normal function	Normal function
0	10	1	00	Coresight (*1)	Tensilica	Normal function
0	10	1	01	Coresight (*1)	SH-X4	Normal function
0	10	1	10	Coresight (*1)	Normal function	Tensilica
0	10	1	11	Coresight (*1)	Normal function	SH-X4
0	11	0	--	SH-X4	Normal function	Normal function
0	11	1	00	SH-X4	Coresight (*1)	Normal function
1	01	0	--	Coresight (*1)	Normal function	Normal function
1	01	1	00	Coresight (*1)	GPS	Normal function
1	01	1	01	Coresight (*1)	SH-X4	Normal function
1	10	0	--	SH-X4	Normal function	Normal function

(*1) "Coresight" is an abbreviation of "Coresight debug port".

2.1.1.10. MD[14:13] Pins — Frequency Mode Setting

These pins select the frequency mode. A crystal oscillator (X6: 20 MHz) is mounted on the RZ/G1M Starter Kit Board.

Do not change the initial setting at shipment (MD14 = 0, MD13 = 1).

MD14	MD13	EXTAL Frequency	EXTAL Divider	PLL1 (CPGM Main)	PLL0 (CPGMC)	PLL3 DDR1600/DDR1333 MD19 = 0/MD19 = 1
0	0	15 MHz	× 1/1	×208 VCO = 3120 MHz	×172 VCO = 1290 MHz	×106/×88 VCO = 1590 MHz/1320 MHz
0	1	20 MHz	× 1/1	×156 VCO = 3120 MHz	×130 VCO = 1300 MHz	×80/×66 VCO = 1600 MHz/1320 MHz
1	0	26 MHz	× 1/2	×240 VCO = 3120 MHz	×200 VCO = 1300 MHz	×122/×102 VCO = 1586 MHz/1326 MHz
1	1	30 MHz	× 1/2	×208 VCO = 3120 MHz	×172 VCO = 1290 MHz	×106/×88 VCO = 1590 MHz/1320 MHz

2.1.1.11. MD19 Pin — Selection of DDR3-SDRAM Bus Clock

This pin selects the frequency of the DDR3-SDRAM bus clock.

MD19	Switching of DDR Clock
0	DDR3-1600 mode
1	DDR3-1333 mode

2.1.1.12. MD28, MD27, and MD22 Pins — Selection of DDR Mode and MTSB Mode

These pins select the DDR3-SDRAM interface mode and MTSB mode.

MD28	MD27	MD22	DDR 64 Bits/ 32 Bits	Remarks	
0	0	0	DDR 64 bits × 1ch	-	
		1	DDR 64 bits × 1ch	-	
	1	0	Reserved	Setting prohibited	
		1	DDR 64 bits × 1ch	User PinMAX	
1	0	0	DDR 32 bits × 1ch	-	
		1	DDR 32 bits × 1ch	-	
	1	0	DDR 32 bits × 1ch	User PinMAX	
		1	DDR 32 bits × 2ch	-	(Fixed)

Note: The MD28, MD27, and MD22 pins are fixed to "1" on the board.

2.1.1.13. MD23 Pin — Selection of SATA0 or USB3.0 Function

This pin selects the SATA0 or USB3.0 function. MD23 is fixed to "0" on the RZ/G1M Starter Kit Board.

MD23	Selection of SATA0 or USB3.0
0	SATA0 (Fixed)
1	USB3.0

2.1.1.14. MD24 Pin — Selection of SATA1 or PCIE Function

This pin selects the SATA1 or PCIE function. MD24 is fixed to "1" on the RZ/G1M Starter Kit Board.

MD24	Selection of SATA1 or PCIE
0	SATA1
1	PCIE (Fixed)

2.1.2. Initial Values of Mode Setting Pins on RZ/G1M Starter Kit Board

Table 2.1.1 Initial Values of RZ/G1M Mode Setting Pins on RZ/G1M Starter Kit Board

MD Pins	Initial Value	Initial Function
MD0	0	Free-running mode
MD[3:1]	010	Boot from QSPI
MD4	0	CS0 space size (64 Mbytes)
MD5	1	Non-secure mode
MD[7:6]	00	Cortex-A15 boot
MD8	0	CS0 space data bus width (16 bits)
MD9	0	Crystal oscillator is used.
MD12	0	-
MD10, MD[21:20], MD11, MDT[1:0]	0,10,0,00	JTAG (CN1) = Boundary SCAN SDHI1 and SDHI2 = Normal function
MD[14:13]	01	Input frequency = 20 MHz
MD19	0	DDR3-1600 mode
MD28, MD27, MD22	111	DDR 32 bits × 2ch
MD23	0	SATA0
MD24	1	PCIE

2.1.3. Multiplexing and Method of Setting for Mode Setting Pins

The following table covers the pin functions that are multiplexed with the mode pins of the RZ/G1M, and how the individual mode pins are set. For the mode pins that are used with fixed values, resistors are used to set them to their fixed values according to the initial settings in table 2.1.1, Initial Values of RZ/G1M Mode Setting Pins on RZ/G1M Starter Kit Board. Such mode pins are described as "Fixed by a resistor" in the Setting Method column in the table below.

Table 2.1.2 Pin Multiplexing of Mode Setting Pins of RZ/G1M

MD Pin	Pin Function	Strapping Options	Setting Method	Default
MD0	DU1_CDE (GPIO)	Free-running (0)/Step-up (1)	Fixed by resistor	Pulled-down (0)
MD1	DU1_DISP	Selects boot device	Fixed by resistor	Pulled-down (0)
MD2	DU1_VSYNC		Fixed by resistor	PULLED-UP(1)
MD3	DU1_HSYNC		Fixed by resistor	Pulled-down (0)
MD4	WE1#	Selects area 0 size	Fixed by resistor	Pulled-down (0)
MD5	AUDIO_CLKOUT (GPIO)	Secure (0) or non-secure (1) mode	Fixed by resistor	PULLED-UP(1)
MD6	WE0#	Selects boot processor	Fixed by resistor	Pulled-down (0)
MD7	DACK0 (GPIO)		Fixed by resistor	Pulled-down (0)
MD8	EX_CS5# (GPIO)	Selects EXBUS width	Fixed by a resistor	Pulled-down (0)
MD9	EX_CS3# (GPIO)	EXTAL or EXTAL/XTAL	Fixed by a resistor	Pulled-down (0)
MD10	BS#	Debugging mode	Fixed by resistor	Pulled-down (0)
MD11	DU1_DB5		Fixed by resistor	Pulled-down (0)
MD12	RD#		Fixed by resistor	Pulled-down (0)
MD13	A3	Selects frequency mode	Fixed by a resistor	Pulled-up (1)
MD14	A19		Fixed by a resistor	Pulled-down (0)
MD15	-	-	-	-
MD16	-	-	-	-
MD17	-	-	-	-
MD18	-	-	-	-
MD19	A14	DDR clock 1600/1333	Fixed by resistor	Pulled-down (0)
MD20	A15	Debugging mode	Fixed by resistor	Pulled-down (0)
MD21	A13		Fixed by resistor(JP9 off)	PULLED-UP(1)
MD22	A10	DDR, MTSB mode	Fixed by a resistor	Pulled-up (1)
MD23	A2	Selects SATA0/USB3.0	Fixed by a resistor	Pulled-down (0)
MD24	A4	Selects SATA1/PCIE	Fixed by a resistor	Pulled-up (1)
MD25	-	-	-	-
MD26	-	-	-	-
MD27	A7	DDR, MTSB mode	Fixed by a resistor	Pulled-up (1)
MD28	A1		Fixed by a resistor	Pulled-up (1)
MDT0	SIM0_CLK	Debugging mode	Fixed by resistor	Pulled-down (0)
MDT1	SIM0_RST		Fixed by resistor	Pulled-down (0)

2.1.4. Block Diagram of Peripheral Circuit for Mode Pins

On the RZ/G1M Starter Kit Board, pull-up (100 k Ω) and pull-down (10 k Ω) resistors are used to implement the settings of the mode pins that are largely used with fixed values. When changes to the settings of mode pins are likely, this can be implemented by switches which, through resistive voltage division, select the low level when turned on and the high level when turned off.

When the RZ/G1M is released from the power-on reset (when the PRESET# signal of the RZ/G1M is changed from low to high), the mode value set by the switch or resistive voltage division is input to the RZ/G1M.

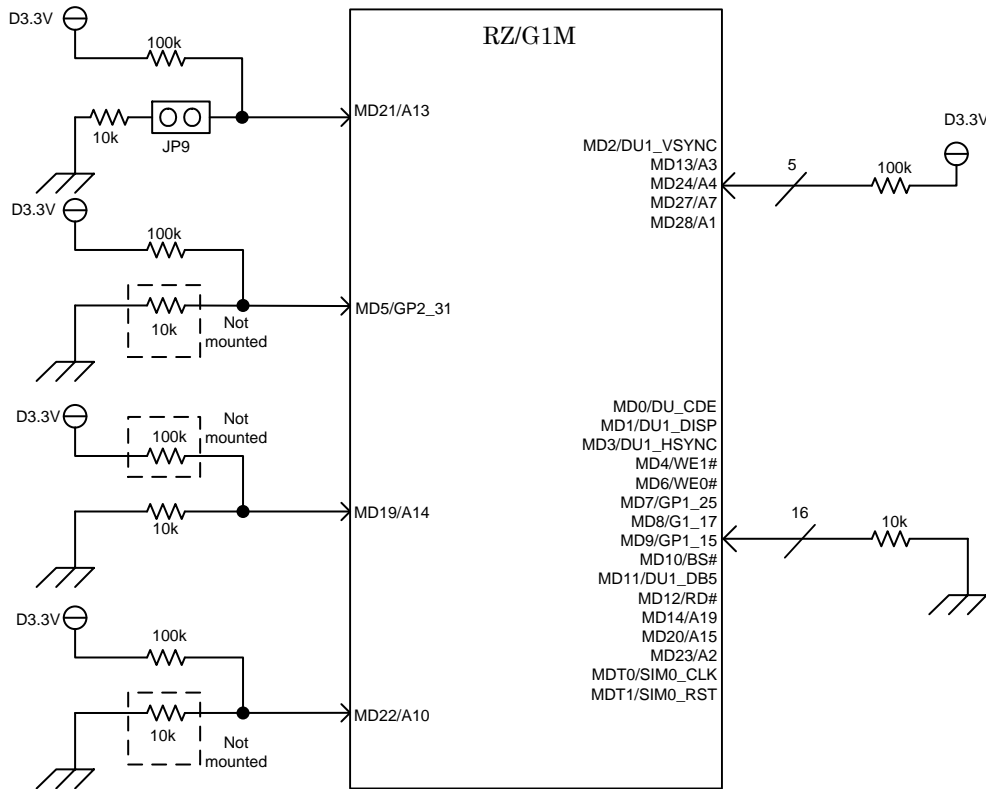


Figure 2.1.1 Peripheral Circuit for Mode Pins on RZ/G1M Starter Kit Board

2.2. DDR3L-SDRAM Interface

2.2.1. Specifications

The RZ/G1M Starter Kit Board incorporates four 4-Gbit DDR3-SDRAMs (16-bit bus width) (DDR: 32 bits × 2 channels) and operates at a maximum speed of DDR3-1600. On the RZ/G1M Starter Kit Board, the RZ/G1M and DDR3-SDRAMs are connected in 32-bit × 2-channel mode; the DDR3-SDRAMs on the channel 0 side are allocated to the address space from H'01_0000 0000 to H'01_3FFF FFFF and those on the channel 1 side are allocated to the address space from H'02_0000 0000 to H'02_3FFF FFFF. The address ranges from H'00_4000 0000 to H'00_7FFF FFFF can be accessed by default as a mirror area of H'01_0000 0000 to H'01_3FFF FFFF.

Table 2.2.1 DDR3L-SDRAM Specifications

Interface	DDR3L-SDRAM
Product name	H5TC4G63AFR-PBA (DDR3-1600, ×16 bits, 4 Gbits) × 4 pcs
Power supply voltage	1.35 V
Capacity	Total: 2 Gbytes, Channel 0: H'01_0000 0000 to H'01_3FFF FFFF Channel 1: H'02_0000 0000 to H'02_3FFF FFFF
Bus width	32-bit data bus × 2ch
Memory bus frequency (RZ/G1M spec.)	DDR3-1600 max.

Note:

To access the address spaces for channels 0 and 1 as a single consecutive area, register settings are necessary. For details, refer to the RZ/G1M documentation.

2.2.2. Signal Correlation

Table 2.2.2 DDR3L-SDRAM Signal Correlation

RZ/G1M (DDR 32 bits × 2ch)	DDR3L-SDRAM			
	Channel 1		Channel 0	
	M1	M2W	M3	M4
	D[31:16]	D[15:0]	D[31:16]	D[15:0]
M1DQ[31:16]	DQU[7:0], DQL[7:0]	-	-	-
M1DQ[15:0]	-	DQU[7:0], DQL[7:0]	-	-
M0DQ[31:16]	-	-	DQU[7:0], DQL[7:0]	-
M0DQ[15:0]	-	-	-	DQU[7:0], DQL[7:0]
M1A[15:0]	A[15:0]	A[15:0]	-	-
M0A[15:0]	-	-	A[15:0]	A[15:0]
M1BA[2:0]	BA[2:0]	BA[2:0]	-	-
M0BA[2:0]	-	-	BA[2:0]	BA[2:0]
M1CK1, M1CK1#	CK, CK#	-	-	-
M1CK0, M1CK0#	-	CK, CK#	-	-
M0CK1, M0CK1#	-	-	CK, CK#	-
M0CK0, M0CK0#	-	-	-	CK, CK#
M1CKE1	CKE	-	-	-
M1CKE0	-	CKE	-	-
M0CKE1	-	-	CKE	-
M0CKE0	-	-	-	CKE
M1CS1#	CS#	-	-	-
M1CS0#	-	CS#	-	-
M0CS1#	-	-	CS#	-
M0CS0#	-	-	-	CS#
M1WE#	WE#	WE#	-	-
M0WE#	-	-	WE#	WE#
M1RAS#	RAS#	RAS#	-	-
M0RAS#	-	-	RAS#	RAS#
M1CAS#	CAS#	CAS#	-	-
M0CAS#	-	-	CAS#	CAS#
M1DQS[3:2], M1DQS[3:2]#	DQSU, DQSL DQSU#, DQSL#	-	-	-
M1DQS[1:0], M1DQS[1:0]#	-	DQSU, DQSL DQSU#, DQSL#	-	-
M0DQS[3:2], M0DQS[3:2]#	-	-	DQSU, DQSL DQSU#, DQSL#	-
M0DQS[1:0], M0DQS[1:0]#	-	-	-	DQSU, DQSL DQSU#, DQSL#
M1DM[3:2]	DMU, DML	-	-	-
M1DM[1:0]	-	DMU, DML	-	-
M0DM[3:2]	-	-	DMU, DML	-
M0DM[1:0]	-	-	-	DMU, DML
M1ODT1	ODT	-	-	-
M1ODT0	-	ODT	-	-
M0ODT1	-	-	ODT	-
M0ODT0	-	-	-	ODT
M1RESET#	RESET#	RESET#	-	-
M0RESET#	-	-	RESET#	RESET#

(*) DDR_VDD/2 [V] is supplied to the M0VREFDQ[1:0] and M1VREFDQ[1:0] pins of the RZ/G1M.

2.2.3. Block Diagram

The following figure shows a block diagram of the DDR3-SDRAM interface.

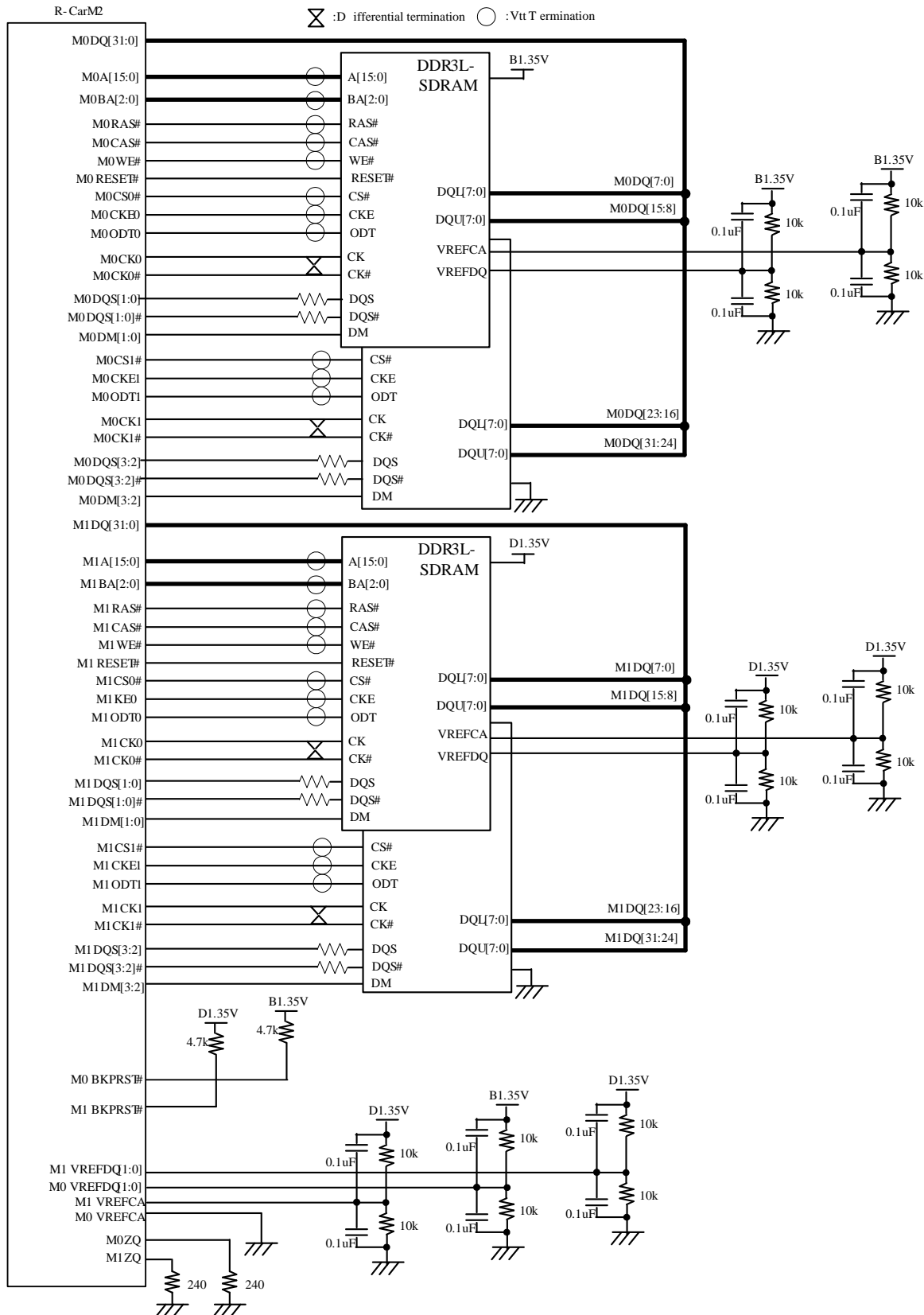


Figure 2.2.1 Block Diagram of DDR3-SDRAM Interface

2.3. SPI-FLASH Interface (QSPI)

2.3.1. Specifications

The RZ/G1M Starter Kit board incorporates 512-Mbit and 32-Mbit SPI flash memory devices manufactured by Spansion. These SPI flash memory devices are connected to the QSPI of the RZ/G1E via jumper JP2. When the 512-Mbit SPI flash memory (U16) is to be accessed, set JP2 to pin 1 side, and when the 32-Mbit SPI flash memory (U579) is to be accessed, set JP2 to the pin 3 side.

Since the loader and mini-monitor are stored in the lower-order address space of the SPI flash memory (U579, 32 Mbits), do not modify the contents of this area. The contents of the SPI flash memory (U16, 512 Mbits) can be modified as required.

Table 2.3.1 Flash Memory Specifications

QSPI controller	RZ/G1M's on-chip QSPI module
SPI flash memory	(1) U16: Spansion S25FL512SAGMFIG11 (512 Mbits) (2) U579: Spansion S25FL032P0XMF1011 (32 Mbits)
Clock rate of RZ/G1M's QSPI	48.75-MHz operation (max.)

2.3.2. Block Diagram

A block diagram of the SPI flash memory interface is shown below.

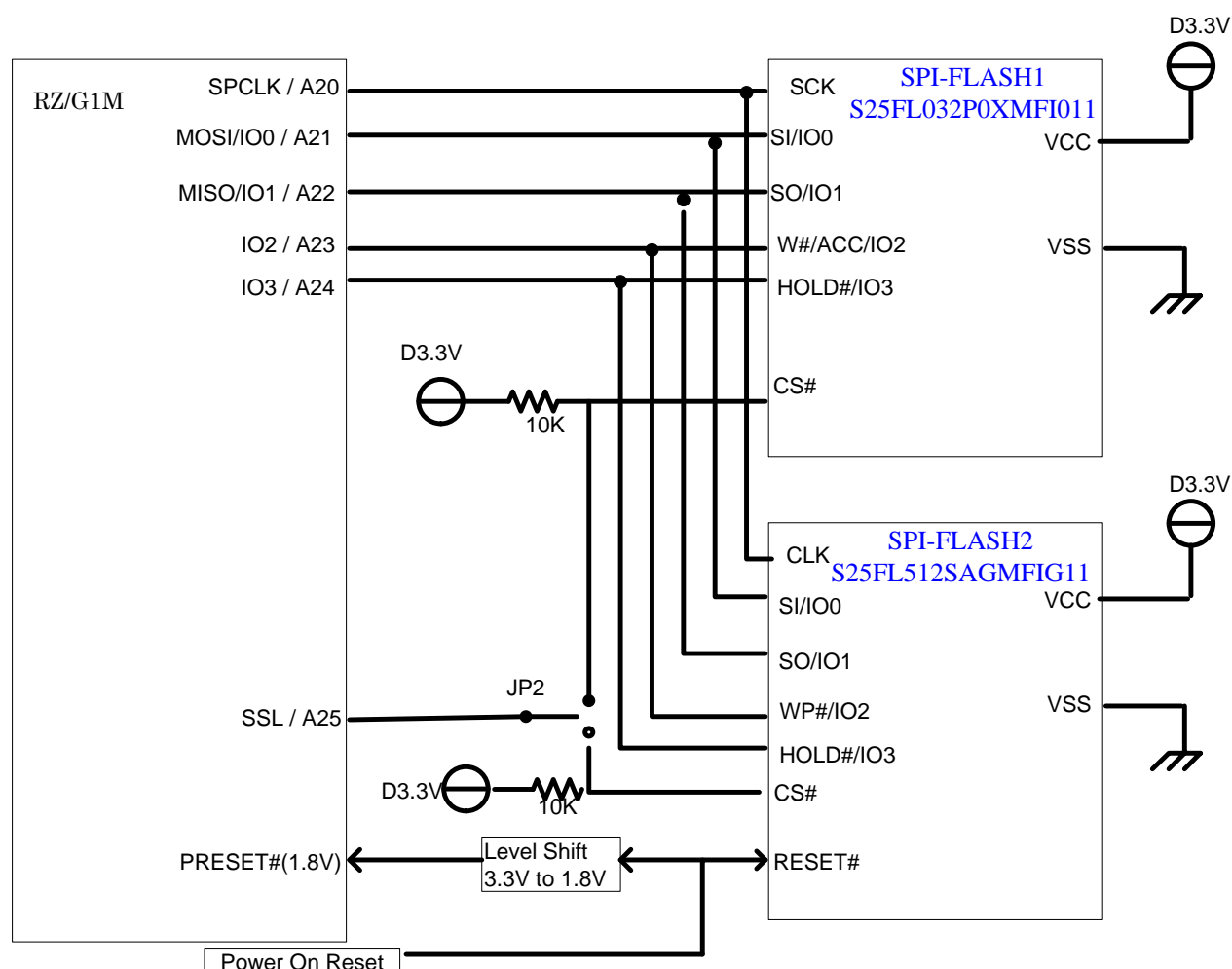


Figure 2.3.1 Block Diagram of SPI-Flash Interface

2.4. Video Input Interface

2.4.1. Specifications

On the RZ/G1M Starter Kit Board, ADV7180WBCP32Z (U22) manufactured by Analog Devices is connected to VIN0 of the RZ/G1M and used as a composite video decoder. The ADV7180WBCP32Z (U22) handles inputs in the ITU-R BT.656 8-bit (YCbCr) format according to the switch settings. The block diagram of the VIN0 interface is shown below.

The registers of ADV7180 should be set via channel 2 of the I2C.

Table 2.4.1 Video Input Specifications

Video input module	RZ/G1M's on-chip video input module channel 0
Composite video decoder for VIN1	U22: ADV7180WBCP32Z by Analog Devices I ² C-BUS ch2 slave address = H'40 for write, H'41 for read
Video input connector	CN: RCA connector for VIN1

2.4.2. Block Diagram

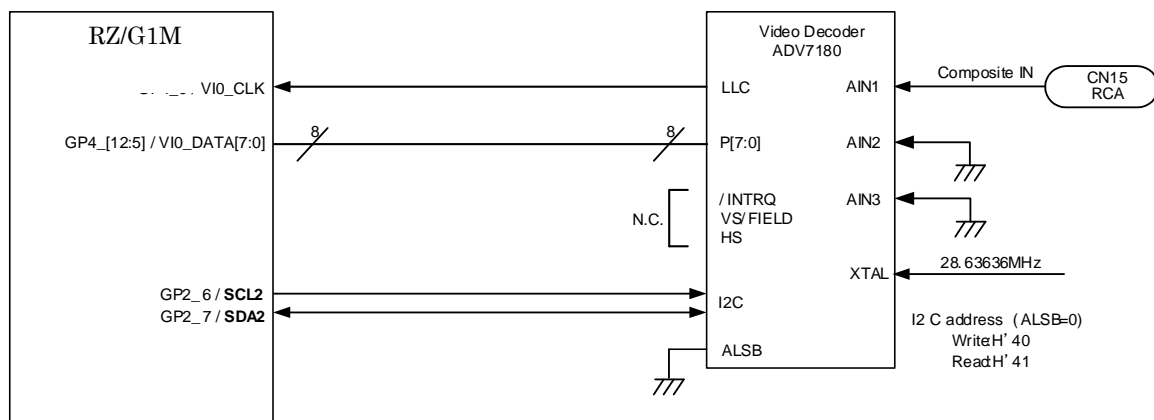


Figure 2.4.1 Block Diagram of Video Input Interface

2.5. Video Output Interface

2.5.1. Specifications

The RZ/G1M Starter Kit Board incorporates one display unit (DU) with the LVDS interface and one display unit with the digital RGB interface.

On the RZ/G1M Starter Kit Board, the HDMI transmitter (ADV7511) converts the digital RGB signals of DU1 to HDMI signals. These digital RGB signals are also connected to the EXIO connector (CN30). In addition, the LCD connector (CN30) is directly connected to DU_LVDS channel 0 (DU0_LVDS).

Table 2.5.1 Video Output Interface Specifications

Display controller	RZ/G1M's on-chip display unit
	[LVDS Output]
DU0_LVDS	Connector CN30: DF14A-20P-1.25H by Hirose, for LVDS signals. CN31: Backlight control and I2C / interrupt input for touch.
	[HDMI Output]
DU1 (digital RGB)	HDMI transmitter converts digital RGB signals to HDMI signals. U44: ADV7511WBSWZ by Analog Devices Connector CN45: HMNF-195N-4BH90 (HDMI type A, standard, 19-pin) by Accurate Innotech

2.5.2. Block Diagram

A block diagram of the video output interface on the RZ/G1M Starter Kit Board is shown below.

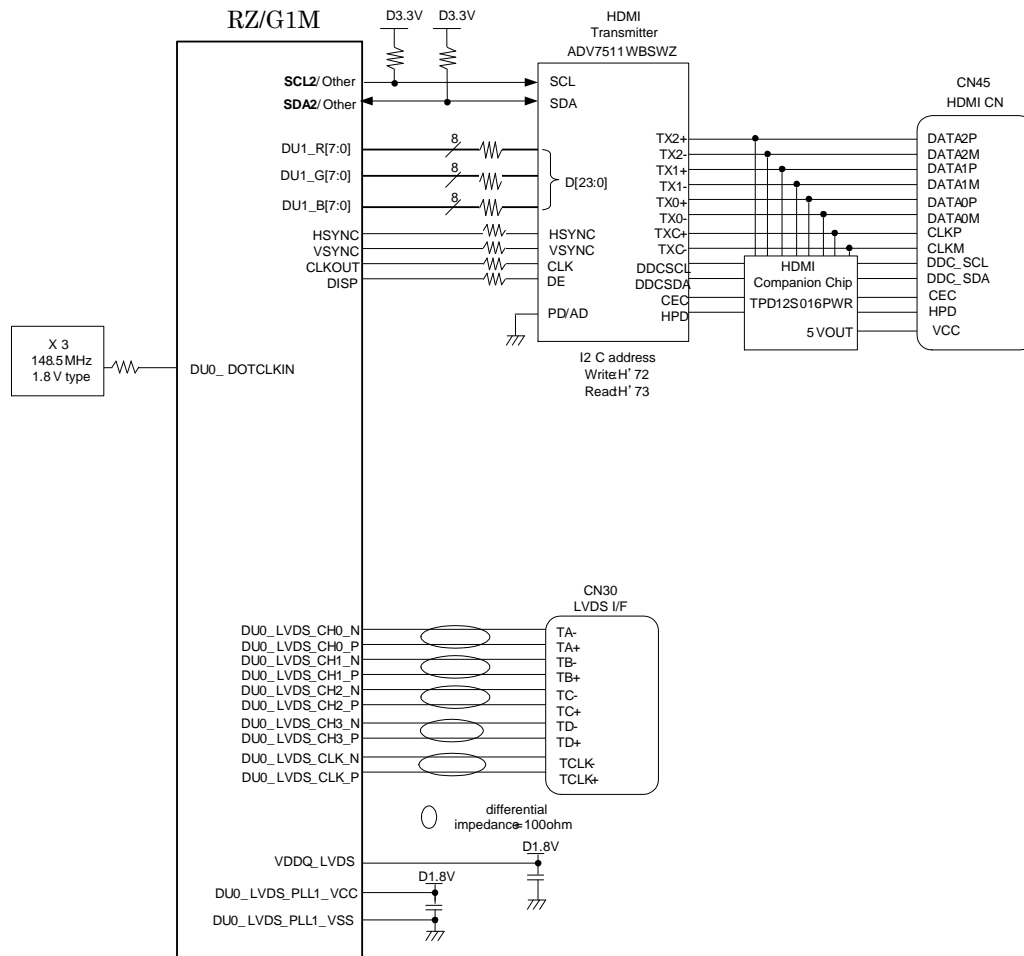


Figure 2.5.1 Block Diagram of Video Output Interface

2.6. Debugger Interface

2.6.1. Specifications

The RZ/G1M Starter Kit Board incorporates a debugger interface via a 20-pin connector (DBG) for connection to the JTAG emulator.

The RZ/G1M supports the DBG3 interface as a debugger interface, but the RZ/G1M Starter Kit Board does not include this function. The signals related to DBG3 (SDHI2) are instead connected to EXIO connector. On the RZ/G1M Starter Kit Board, the debugging function can be accessed through the JTAG connector CN1

(Attention) If use as ARM Coresight debug port, remove JP9 jumper off.

Table 2.6.1 DBG Specifications

DBG interface (20-pin)	CN1: HTST-110-01-S-DV by Samtec
------------------------	---------------------------------

2.6.2. Block Diagram

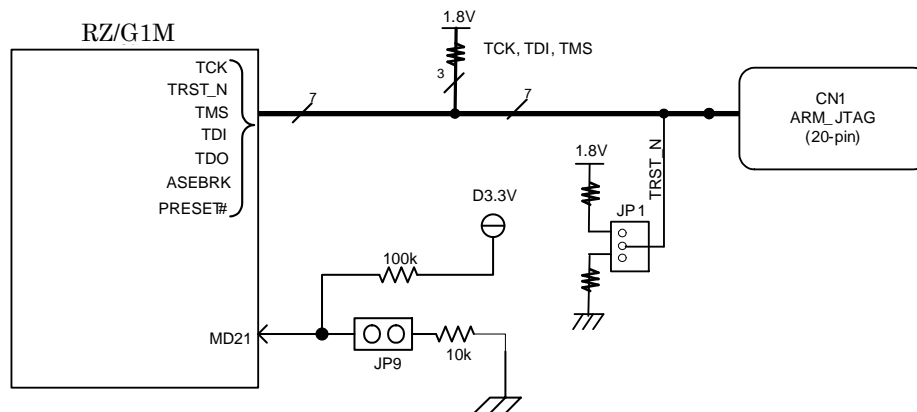


Figure 2.6.1 Block Diagram of JTAG (DBG) Interface

2.7. Debug Ether Interface (EtherMAC)

2.7.1. Specifications

The RZ/G1M Starter Kit Board incorporates the EtherMAC that supports 100Base-T or 10Base-T compliant with IEEE 802.3u. On the RZ/G1M Starter Kit Board, the EtherMAC signals are connected to the RMII PHY interface (KSZ8041RNLI) manufactured by Micrel. In addition, CN3 on the bottom of the board supports the REACH interface sub boards.

Table 2.7.1 Debug Ether Interface Specifications

MAC layer	RZ/G1M's on-chip EtherMAC
Physical layer transceiver	U21: KSZ8041RNLI (RMII) by Micrel
Reach connector	CN3 (as EtherAVB)
Modular connector	CN10: CWKRJ-13BNL (RJ-45 with pulse transformer) by CWE

2.7.2. Block Diagrams

A block diagram of the debug Ether interface is shown below.

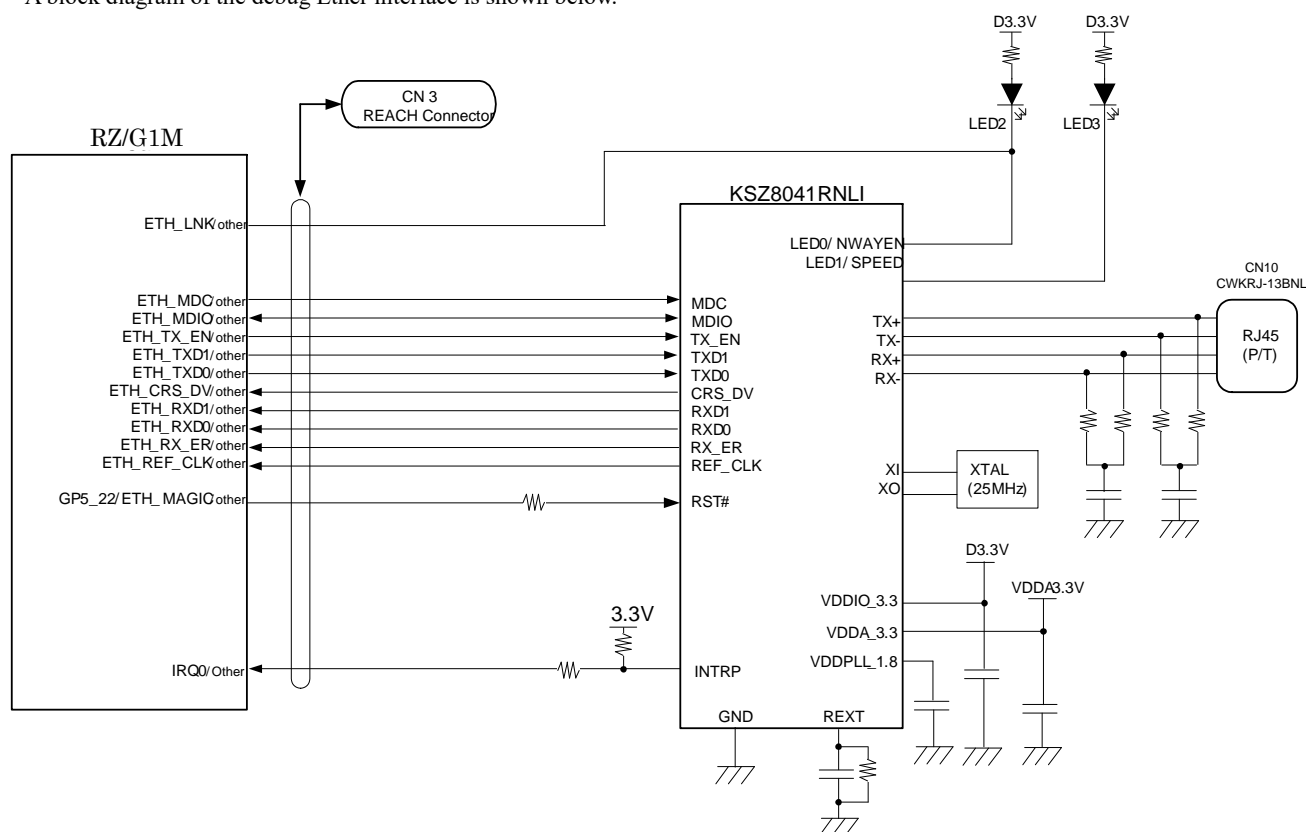


Figure 2.7.1 Block Diagram of Debug Ether Interface

2.8. Audio Codec Interface (SSI0, SSI1, SSI2, and SSI9)

2.8.1. Specifications

On the RZ/G1M Starter Kit Board, the codec (AK4642EN) is connected to the SSI0 and SSI1 of the RZ/G1M. The PDN (power-down) pin of AK4642EN is controlled by the PRESETOUT# signal output from the RZ/G1M.

The audio interface of AK4642EN is in the slave mode after PRESETOUT# is released from a reset and can be switched to the master mode by a register that is accessed via channel 2 of the I²C. Furthermore, the SSI on the RZ/G1M side can be set as the master or a slave. It is assumed that SSI_SDAT0 is set to transmit mode and SSI_SDAT1 is set to receive mode on the RZ/G1M Starter Kit Board.

Among the signals of the audio interface, the signals of SSI0, SSI1, SSI2, and SSI9 are also connected to HDMI transmitter ADV7511 (U44) on the RZ/G1M Starter Kit Board.

Table 2.8.1 SSI Codec Specifications

Controller	RZ/G1M's on-chip SSI0 and SSI1
Codec	U24: AK4642EN by Asahi Kasei
Audio interface	RZ/G1M (SSI) = Master or slave selectable AK4642EN = Master or slave selectable (default: slave)
Audio connector	LINE-OUT CN13, 3.5-mm green mini-jack LINE-IN/MIC-IN CN14 3.5-mm pink mini-jack)

2.8.2. Block Diagram

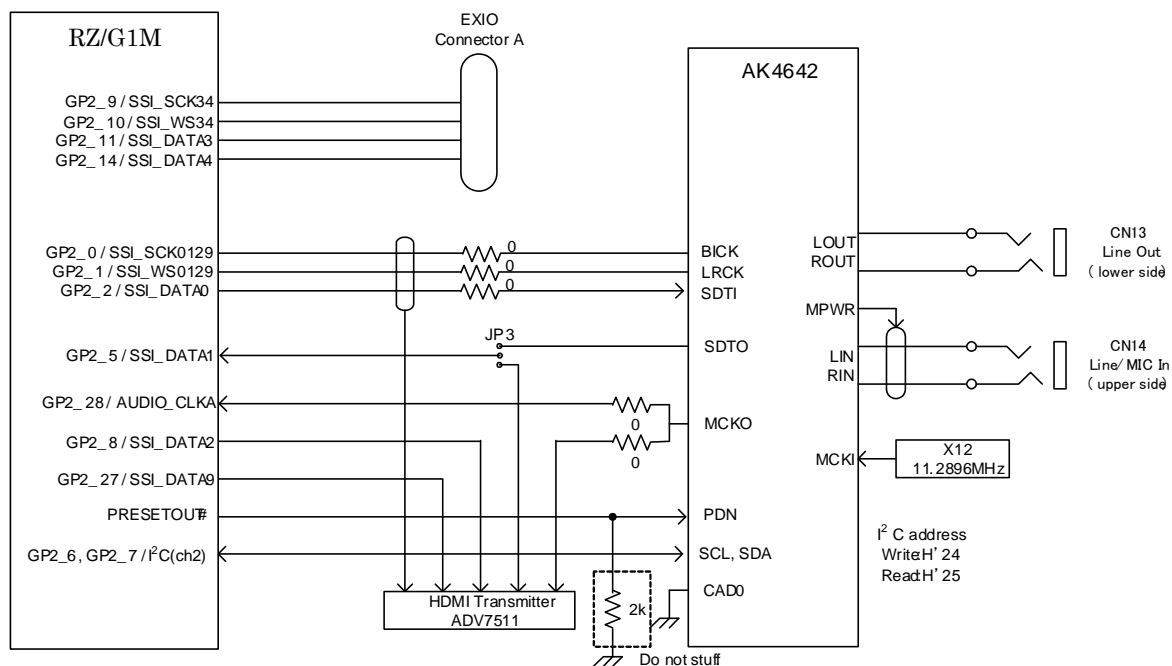


Figure 2.8.1 Block Diagram of Audio Codec Interface

2.9. PCI-Express Interface

2.9.1. Specifications

The RZ/G1M Starter Kit Board incorporates the PCI-Express interface for one lane (×1) as a dedicated interface for the PCI-Express bus. The on-chip PCIE module in the RZ/G1M works in either of two modes, Root Port or Endpoint, which are defined in the PCI Express specifications. In the RZ/G1M, the operating mode is specified through internal register settings (mode setting register (PCIEMSR)). For details, refer to the RZ/G Series User's Manual:Hardware.

Note:

To reduce the difference in wiring length between each pair of differential signals from the RZ/G1M to the PCI-Express slot, the D+ and D- line automatic swap function is used to swap the TODP1_PCIE and TODN1_PCIE signals output from the transmit pins before connection to the slot.

Table 2.9.1 PCI-Express Interface Specifications

PCI-Express controller	RZ/G1M's on-chip PCI-Express controller
PCI-Express slot (1 lane)	JPCIE-4CEE36XRT110by Weknowtechnology (CN5)
PCI-Express clock source	IDT5V41066PGGI by IDT

2.9.2. Block Diagram

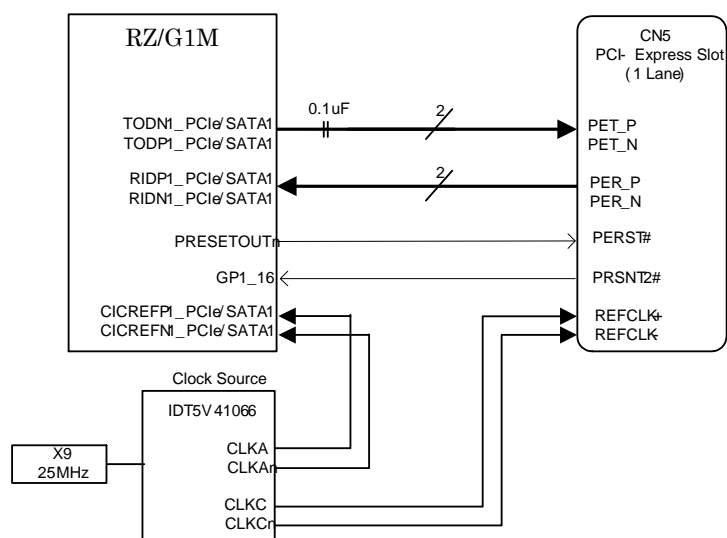


Figure 2.9.1 Block Diagram of PCI-Express Interface

2.10. Serial-ATA Interface

2.10.1. Specifications

The RZ/G1M Starter Kit Board incorporates one serial-ATA interface (SATA0) channel. The RZ/G1M's on-chip serial-ATA interface conforms to the Serial ATA standard rev. 3.1 and supports transfer rates of 1.5 Gbps (Gen1) and 3.0 Gbps (Gen2). The RZ/G1M Starter Kit Board incorporates a 4-pin power connector (CN2) for the ATAPI device. The power connector conversion cable (4-pin to 15-pin) is required to supply power to the SATA device.

Table 2.10.1 Serial-ATA Interface Specifications

Serial-ATA interface controller	RZ/G1M's on-chip serial-ATA controller
Serial-ATA connector (signal)	HSAT-M07-V5D-40 by HON KON (CN4)
Serial-ATA clock source	IDT5V41066PGGI by IDT

2.10.2. Block Diagram

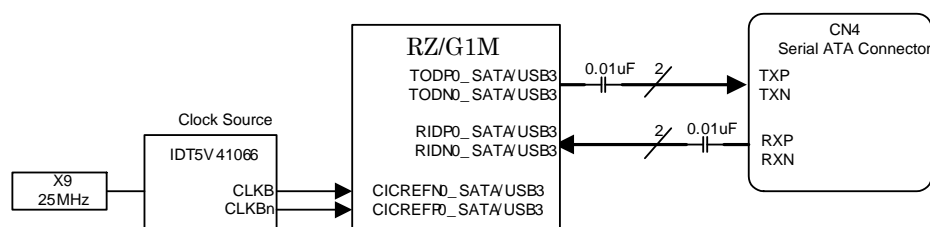


Figure 2.10.1 Block Diagram of Serial-ATA Interface

2.10.3. PCI-Express and Serial-ATA Clock Source Unit

The details on the clock source unit of the PCI-Express interface and serial-ATA interface are shown below. IDT5V41066PGGI manufactured by IDT is used for the clock driver. This clock driver multiplies the input frequency (25 MHz) to supply a 100-MHz differential clock to the RZ/G1M and PCI-Express slot.

Note:

To reduce the difference in wiring length between each pair of differential signals from the RZ/G1M to the clock source, the P and N lines from the clock pins (CICREFP0_SATA/PCIe_18 and CICREFN0_SATA/PCIe_18 signals) are swapped before connection to the clock source.

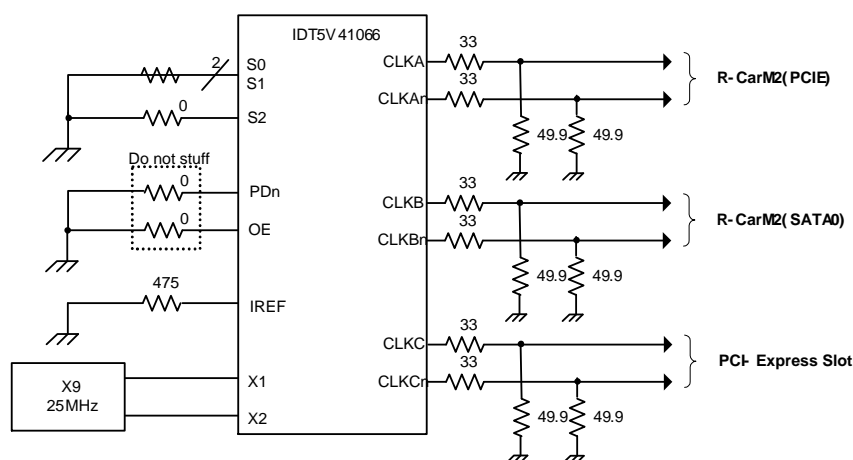


Figure 2.10.2 Block Diagram of PCI-Express and Serial-ATA Clock Source

2.11. SD Card Host Interface 0 (SDHI0)

2.11.1. Specifications

The RZ/G1M Starter Kit Board incorporates an SD card slot (CN8) for the on-chip SD card host interface (SDHI0) of the RZ/G1M. For details on the SDHI0, see the RZ/G Series User's Manual: Hardware.

On the RZ/G1M Starter Kit Board, the interface voltage (VCCQ_SD0) of the SD card slot can be selected by GP2_12. When GP2_12 is set to 1, 3.3 V is supplied as VCCQ_SD0. When GP2_12 is set to 0, 1.8 V is supplied as VCCQ_SD0.

Table 2.11.1 SD Card Host Interface (SDHI0) Specifications

SD card host interface	RZ/G1M's on-chip SD card host interface channel 0 (SDHI0)
Interface voltage control	VCCQ_SD0 = 3.3 V (GP2_12 = '1') VCCQ_SD0 = 1.8 V (GP2_12 = '0')
SD card slot	SDC009-A0-0003 by PROCONN (CN8)

2.11.2. Block Diagram

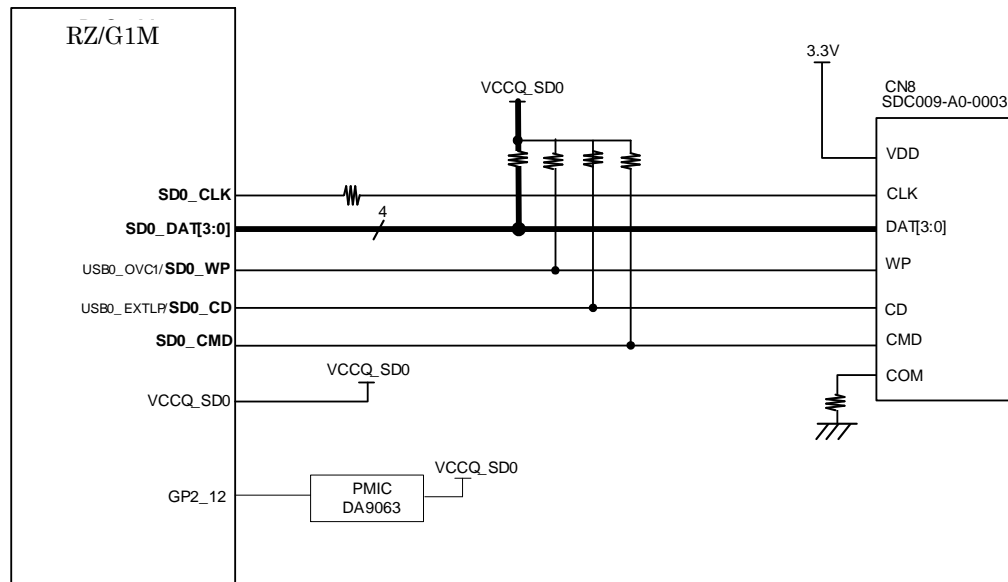


Figure 2.11.1 Block Diagram of SD Card Host Interface (SDHI0)

2.12. SD Card Host Interface 2 (SDHI2)

2.12.1. Specifications

The RZ/G1M Starter Kit Board incorporates a microSD card slot (CN9) for the on-chip SD card host interface (SDHI2) of the RZ/G1M. For details on the SDHI2, see the RZ/G Series User's Manual:Hardware.

On the RZ/G1M Starter Kit Board, the interface voltage (VCCQ_SD2) of the microSD card slot can be selected by GP2_26. When GP2_26 is set to 1, 3.3 V is supplied as VCCQ_SD2. When GP2_26 is set to 0, 1.8 V is supplied as VCCQ_SD2.

Table 2.12.1 SD Card Host Interface (SDHI2) Specifications

SD card host interface	RZ/G1M's on-chip SD card host interface channel 2 (SDHI2)
Interface voltage control	VCCQ_SD2 = 3.3 V (GP2_26 = '1') VCCQ_SD2 = 1.8 V (GP2_26 = '0')
microSD card slot	MSPN09-A0-1002 by PROCONN (CN9)

2.12.2. Block Diagram

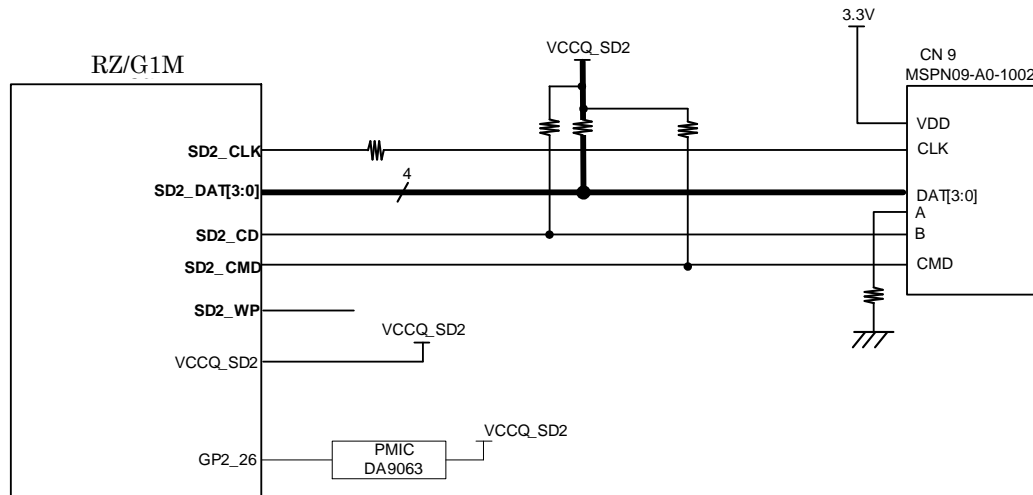


Figure 2.12.1 Block Diagram of SD Card Host Interface (SDHI2)

2.13. USB2.0 Interface

2.13.1. Specifications

The RZ/G1M Starter Kit Board has two USB2.0 ports that can be used as two USB2.0 host interface ports or one USB2.0 host interface port and one USB2.0 function interface port. The function interface is supported in channel 0. The RZ/G1M Starter Kit Board incorporates a micro-AB connector as CN22 and a type A connector as CN7. For details, see the USB specifications in the RZ/G Series User's Manual:Hardware and related datasheets.

Table 2.13.1 USB2.0 Specifications

USB controller	RZ/G1M's on-chip USB2.0 host and function controller
USB power supply	BD6516F by ROHM Current limit: 2.4 [A]
USB host CN	RZ/G1M USB CH1 CN7: Type A connector 67643-3911 by Molex
USB host/function CN	RZ/G1M USB CH0 CN22: micro-AB connector KS-MCR-AB01N3- by Weknowtechnology
ESD protection diode	HZD6.2Z4 by Renesas
Common mode filter	DLP11SN900HL2 by Murata
Chip beads	BLM18PG330SN1D by Murata

* The connector for channel 0 of the USB in the RZ/G1M Starter Kit Board is a mini connector shared by the USB host and function.

2.13.2. Block Diagram

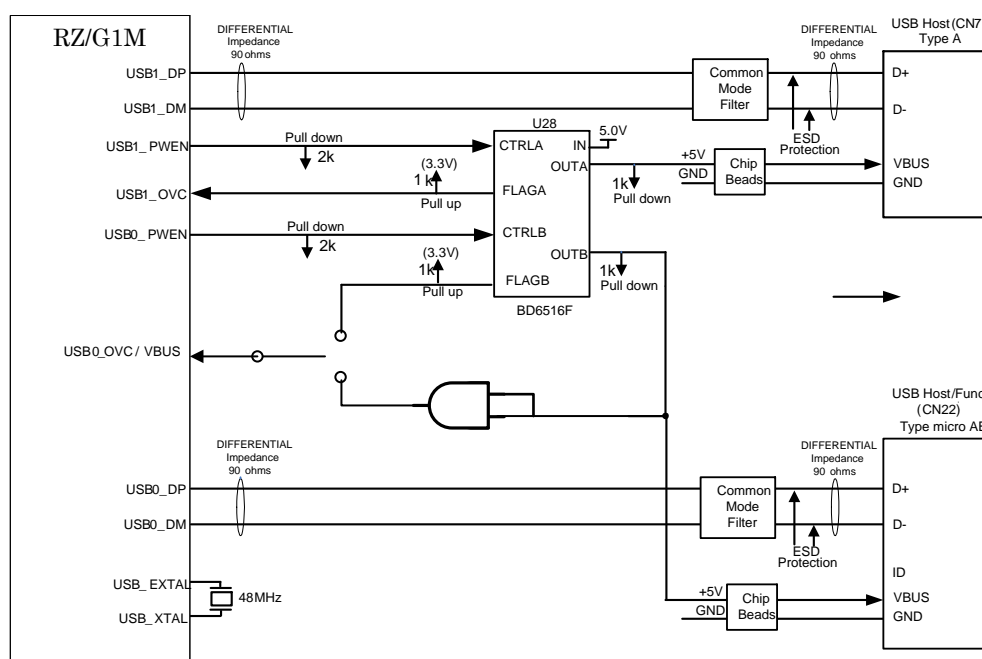


Figure 2.13.1 Block Diagram of USB2.0 Interface

2.14. Debug Serial Interfaces (SCIF0)

2.14.1. Specifications

On the RZ/G1M Starter Kit Board, the SCIF0 (port D) of the RZ/G1M are used as debug serial interface. The SCIF0 of the RZ/G1M is connected to the USB micro-AB connector (CN18) via the USB to UART bridge CP2102. By connecting CN18 to the host PC through a USB cable, this interface can be used as debug serial interface.

The SCIF0 has the features shown below. For details, see the SCIF specifications in the RZ/G Series User's Manual: Hardware.

- Asynchronous serial communications
- Full-duplex communication supported
- Selectable bit rates by using the RZ/G1M's on-chip baud-rate generator

The host PC connected to the RZ/G1M Starter Kit Board requires the CP2102 USB driver software. This driver software can be obtained from the following URL.

<http://www.silabs.com/products/mcu/Pages/USBtoUARTBridgeVCPDrivers.aspx>

Table 2.14.1 Debug Serial Interface Specifications

Serial controller	RZ/G1M's on-chip SCIF0 (port D)
USB to UART bridge	CP2102 (1 Mbps max.) by Silicon Laboratories
Connector	CN18: SCIF0, KS-MCR-B02T3-L by Weknowtechnology

2.15. Reset

2.15.1. Specifications

In the RZ/G1M Starter Kit Board specifications, the power-on reset signal is cleared by the reset IC MAX708SCSA, 200 ms after the 3.3-V power supply has settled. The power supplies for other voltage levels, 12.0 V, 5.0 V, 1.8 V, 1.5 V, and 1.0 V, are not monitored.

A power-on reset signal can be generated by pushing the push switch (SW9). The reset signal is level-shifted from 3.3 V to 1.8 V by the HD74ALVC1G07 and is input to the PRESET# pin of the R- CarM2.

Table 2.15.1 RESET Specifications

	MAX708SCSA by Maxim Integrated
Reset IC	<ul style="list-style-type: none"> • Threshold voltage: 2.93 V • Reset delay time: 200 ms

2.15.2. Block Diagram

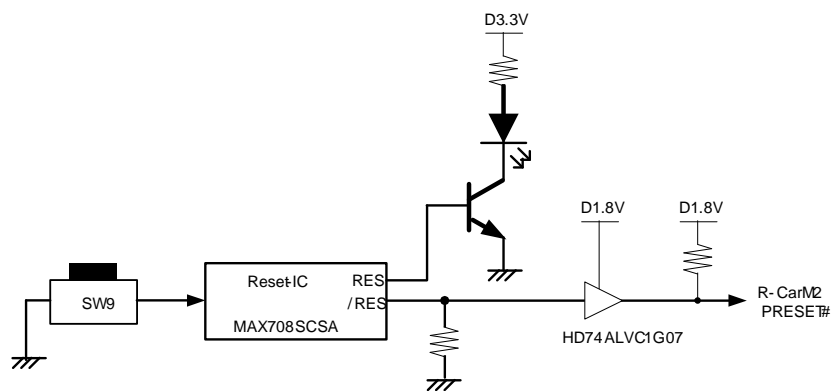


Figure 2.15.1 Block Diagram of Reset Circuit

2.16. I²C Interface

2.16.1. Specifications

The RZ/G1M incorporates seven I²C interface channels. Channels 5 and 6 are 1.8-V interfaces and channels 0 to 4 are 3.3-V interfaces. The following devices are connected to each channel of the I²C interfaces on the RZ/G1M Starter Kit Board.

Table 2.16.1 I²C Interface Specifications

I ² C controller	RZ/G1M's on-chip I ² C controller [1.8 V]
I ² C devices through I ² C (ch5)	CN23: External IO Connector [1.8 V]
I ² C devices through I ² C (ch6)	U37: DA9063 by Dialog Semiconductor U38: DA9210 by Dialog Semiconductor [3.3 V]
I ² C devices through I ² C (ch4)	CN31: Touch screen connector [3.3 V]
I ² C devices through I ² C (ch2)	U44: ADV7511WBSWZ by Analog Devices U22: ADV7180WBCP32Z by Analog Devices U24: AK4642EN by AKM Semiconductor U50: R1EX24002ATAS0 by Renesas
I ² C devices through I ² C (ch1 port E)	U55: DA9063 by Dialog Semiconductor

2.17. External Interrupts

2.17.1. Specifications

The RZ/G1M has external interrupt input pins NMI, IRQ[9:0], INTC_IRQ[4:0]#, and INTC_EN[1:0]#. The RZ/G1M Starter Kit Board uses IRQ0, IRQ1, and IRQ2 as external interrupt input pins. It also uses GP3_29 and GP6_29 as GPIO interrupts. These pins should be used as active-low signals in programs. For the interrupt functions of the RZ/G1M, see the RZ/G Series User's Manual:Hardware.

The devices and connectors of the interrupt request sources on the RZ/G1M Starter Kit Board are shown below.

Table 2.17.1 External Interrupt Specifications

Interrupt Pin	Devices that Output Interrupt Request	Connectors
IRQ0	RMII PHY U21: KSZ8041RNL1 by Micrel	
IRQ1	Touch Screen	CN31: GB10BXHAMLFSNP
IRQ2	PMIC U55: DA9063 by Dialog Semiconductor	
GP3_29	HDMI transmitter U44: ADV7511WBSWZ by Analog Devices	
GP6_29	Clock Synchronized Serial Device	CN6: 6-pin header

2.17.2. Block Diagram

A block diagram of external interrupts is shown below.

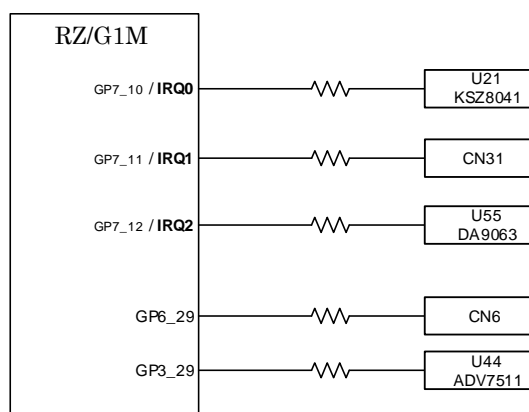


Figure 2.17.1 Block Diagram of External Interrupts

2.18. PWM

The RZ/G1M incorporates a seven-channel pulse width modulation timer (PWM). On the RZ/G1M Starter Kit Board, the use of other pin functions is given priority over the PWM functions in the case of pins that have multiplexed PWM functions. See the table below for details.

Table 2.18.1 Pin Functions Given Priority over PWM Functions

PWM	Pin Functions Given Priority over PWM Functions
PWM0	SD1_CD to SDHI1 interface
PWM0_B	GPIO (GP5_30)
PWM1	Mode pin 'MD8'
PWM1_B	SD1_WP to SDHI1 interface
PWM2W	LBSC 'BS#'
PWM2W_B	LBSC address 'A0'
PWM3	GPIO (GP1_24)
PWM4	GPIO (GP3_26)/DU1_DOTCLKOUT1
PWM4_B	Mode pin 'MD0'
PWM5	GPIO (GP7_21)
PWM5_B	GPIO (GP7_20)
PWM6	GPIO (GP7_22)

2.19. Clock

The RZ/G1M Starter Kit Board uses the crystal oscillators and resonators shown below.

2.19.1. Clocks Supplied to the RZ/G1M

Table 2.19.1 List of Clocks and Crystals for RZ/G1M

No.	Xn	Frequency	Pin Name on RZ/G1M	Type	Remarks
1	X1	48.0000 MHz	USB_XTAL, USB_EXTAL	Resonator	-
2	X16		DU1_DOTCLKIN	(Oscillator, not installed)	3.3V
3	X3	148.500 MHz	DU0_DOTCLKIN	Oscillator	1.8V
4	X4		SCIF_CLK	(Oscillator, not installed)	3.3V
5	X7	20.0000 MHz	EXTAL	Oscillator	1.8V

2.19.2. Clocks Supplied to Devices Other than RZ/G1M

Table 2.19.2 List of Clocks and Crystals Other than for RZ/G1M

No.	Xn	Frequency	Device	Device Pin Name	Type
1	X9	25.0000 MHz	IDT5V41066	X1, X2	Resonator
2	X8	25.0000 MHz	KSZ8041RNLI	XI, XO	Resonator
3	X13	12.0000 MHz	ADV7511WBSWZ	CEC_CLK	Oscillator
4	X11	28.63636 MHz	ADV7180WBCP32Z	XTAL	Oscillator
5	X14	11.2896 MHz	AK4642	MCKI	Oscillator
6	X10	74.25MHz	SG-8002CE	CAN_CLK	Oscillator
7	X12	74.25MHz	SG-8002CE	IECLK_B	Oscillator
8	X15	74.25MHz	SG-8002CE	AVB_GTXREFCLK	Oscillator

2.20. Power Supply

2.20.1. Specifications

The RZ/G1M Starter Kit Board operates on a single 12.0-VDC power supply. The power supplies used for the RZ/G1M Starter Kit Board are generated by the switching regulators and low-dropout regulators.

Specified sequences should be used to turn on and off the power supply to the RZ/G1M. Be sure to control the ACC switch (SW26) to obey the power sequence on the RZ/G1M Starter Kit Board.

See the table below for regulators used to generate power supplies on the RZ/G1M Starter Kit Board, their input voltage (V_{in}) and output voltage (V_{out}), and whether the ACC switch can be used to enable or disable output of power supplies.

Table 2.20.1 List of RZ/G1M Starter Kit Board Switching Controllers and Regulators

V_{in}	V_{out}	Switching Controller and Regulator	ACC Switch Control
Power Supply 12.0 VDC through CN25	D12.0V	-	Not supported
D12.0V	D5.0V / VSYS	IR 3838 (U576)	Supported
D5.0V	VTT	Dialog Semiconductor DA9063 (U55)	Supported
	D1.8V	Dialog Semiconductor DA9063 (U55)	Supported
	D1.0V	Dialog Semiconductor DA9063 (U55)	Supported
	D1.35V	Dialog Semiconductor DA9063 (U55)	Supported
	D3.3V	Dialog Semiconductor DA9063 (U55)	Supported
	D1.8V_PERI	Dialog Semiconductor DA9063 (U55)	Supported
	VCCQ1.8V	Dialog Semiconductor DA9063 (U55)	Supported
	VLDO3_SD0 (3.3 / 1.8 V)	Dialog Semiconductor DA9063 (U55)	Supported
	VLDO4_SD1 (3.3 / 1.8 V)	Dialog Semiconductor DA9063 (U55)	Supported
	VIO33 (3.3 V)	Dialog Semiconductor DA9063 (U55)	Supported
	VLDO7_1.8V	Dialog Semiconductor DA9063 (U55)	Supported
	VLDO8_SD2 (3.3 / 1.8 V)	Dialog Semiconductor DA9063 (U55)	Supported
	DVFS1.0V	Dialog Semiconductor DA9210 (U56)	Supported

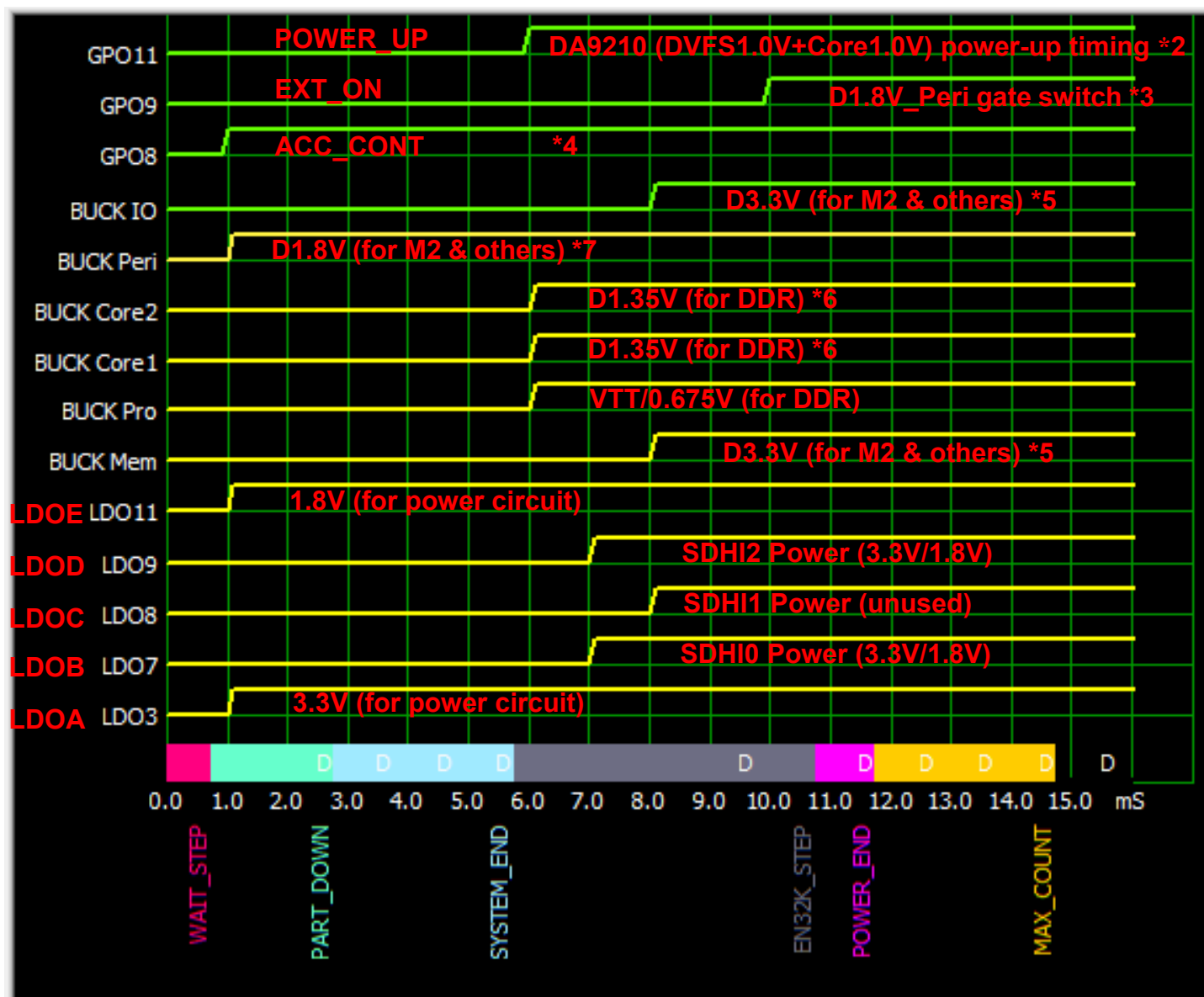
[Note]

As D12.0V is output to the following connectors, connecting or disconnecting an external board or a cable to these connectors must be performed while 12 V is not supplied to CN25 (while the 120-VAC switch is off).

- Power supply connector for serial-ATA interface (CN4)
- Connector for PCI Express (CN5)
- Back Light Header Connector (CN31)

2.20.2. Power-On Sequence

The diagram of the sequence for turning on the power (DA9063L-6B) for the RZ/G1M Starter Kit Board Rev2.0 is shown below.



- *1 In the power-off sequence, turn off the power supplies in reverse order of the power-on sequence.
- *2 The Co-PMIC (DA9210: DVFS1.0V and Core1.0V) are turned on/off with this 'POWER_UP' timing.
- *3 'EXT_ON' signal controls U581(MOS-SW: NX3P1108) to turn on/off D1.8V_Peri(ADV7511, ADV7180etc)
- *4 'ACC_CONT' signal is used with other control signals to turn on/off 5V(VSYS).
In the power-off sequence, 'ACC_CONT' keep 5V turn on.
- *5 BUCKIO and BUCKMem are merge mode.
- *6 BUCKCore1 and BUCKCore2 are merge mode.
- *7 BUCKPeri provide D1.8V including VCCQ_ISO and D1.8V_Peri

Figure 2.20.1 Power-On Sequence

3. Outline Diagrams of RZ/G1M Starter Kit Board

3.1. External Dimensions and Hole Locations of RZ/G1M Starter Kit Board

The following shows the external dimensions and hole locations of the RZ/G1M Starter Kit Board. (Unit: mm)

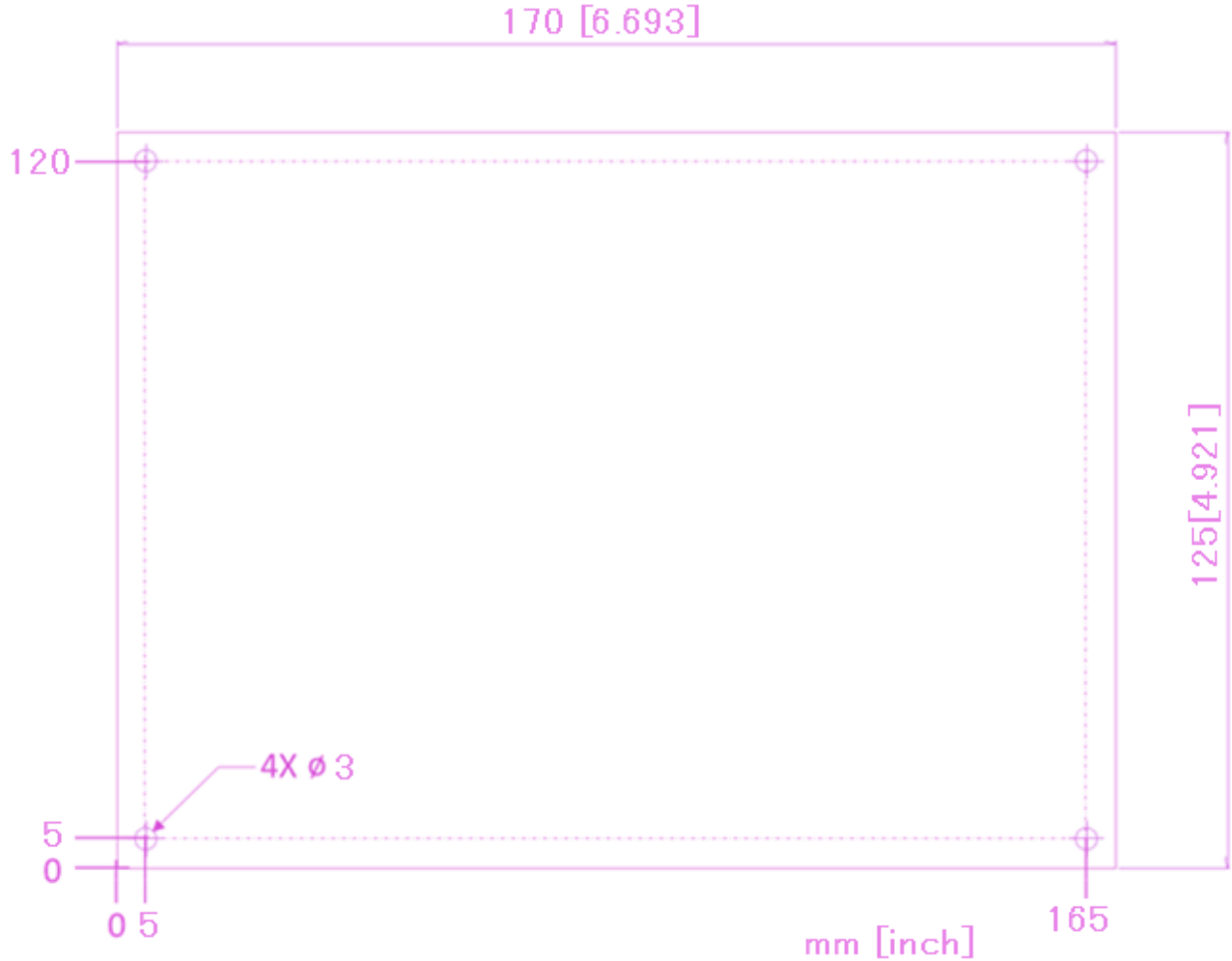


Figure 3.1.1 External Dimensions and Hole Locations of the RZ/G1M Starter Kit Board
(Top View)

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3.2. Connector Locations on RZ/G1M Starter Kit Board (Component Surface)

The following shows the connector locations on the component surface.

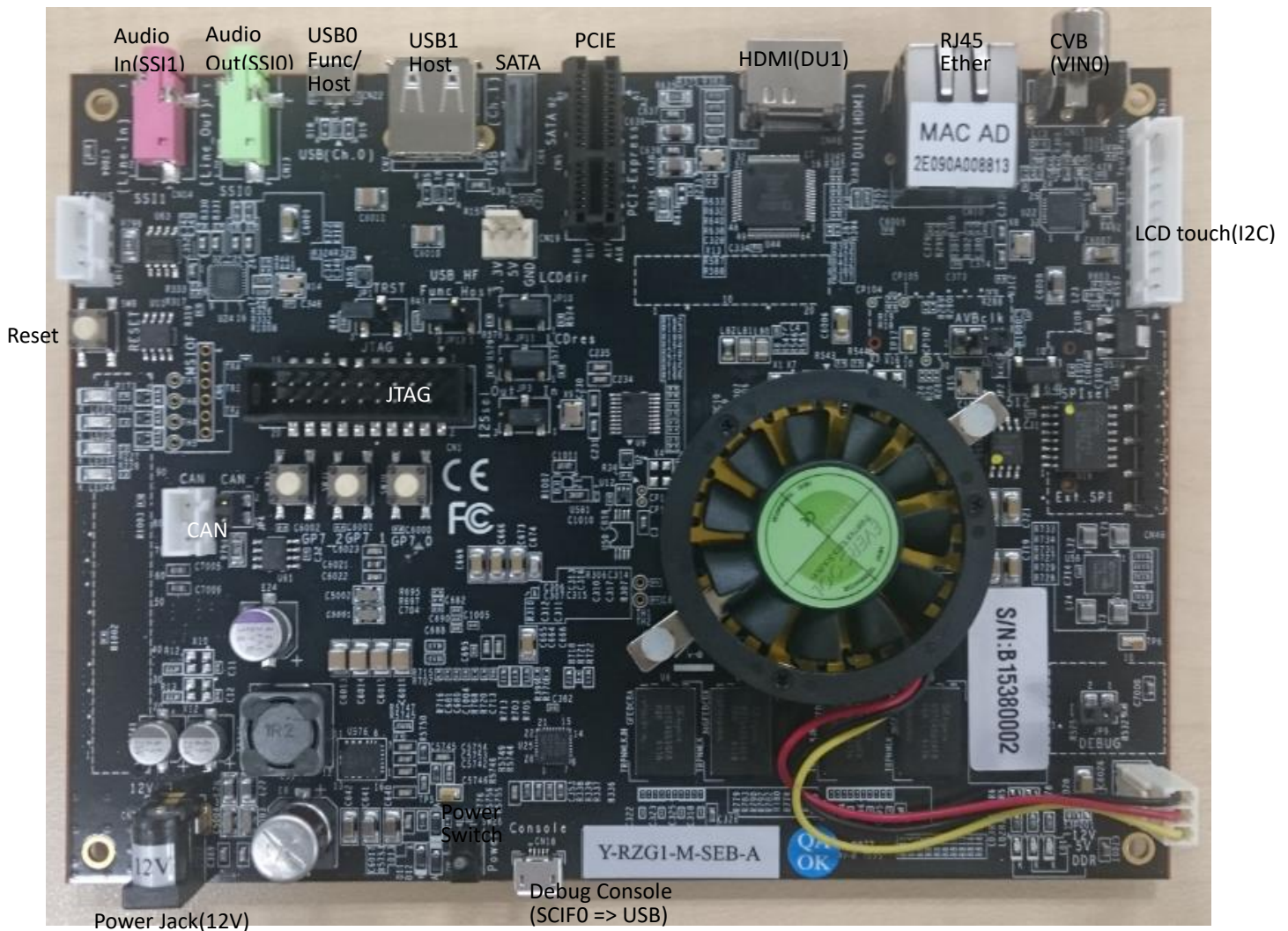
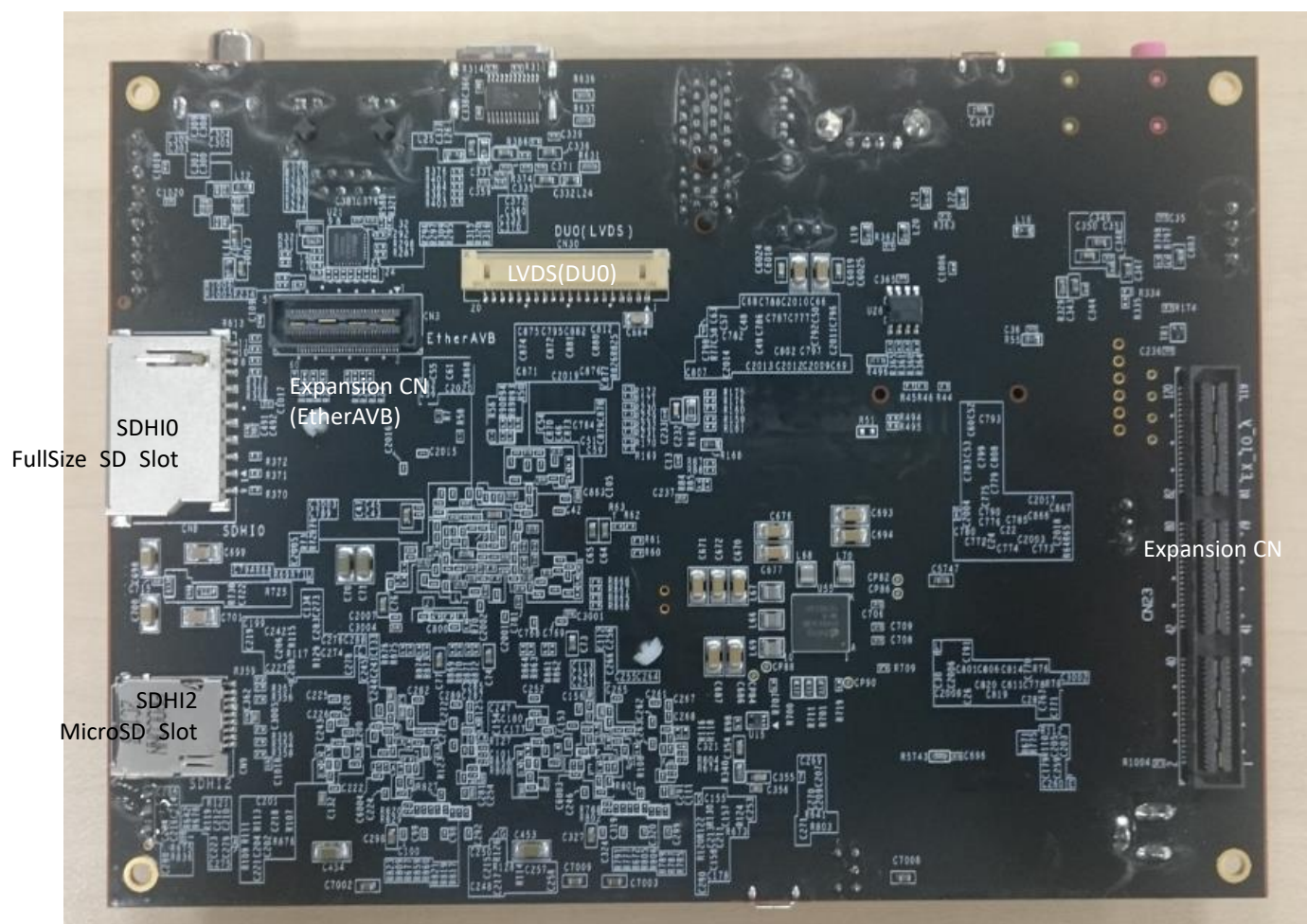


Figure 3.2.1 Connector Locations of the RZ/G1M Starter Kit Board (Component Surface)
(Top View)

a

3.3. Connector Locations on RZ/G1M Starter Kit Board (Solder Surface)

The following shows the connector locations on the solder surface.



**Figure 3.3.1 Connector Locations of the RZ/G1M Starter Kit Board (Solder Surface)
(Bottom View)**